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Phone: (818) 488-8143
Fax: (818) 332-4205

Send to: NGUYEN, Duc M.	**From: Mariana Paula Noli**
Company: USPTO	Date: January 21, 2009
Fax Number: (571) 273-8300	Phone No.: (818) 488-8143

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Total pages, including cover: 26

Comments:

Applicant: SiRF Technology, Inc.
Title: "SERIAL RADIO FREQUENCY TO BASEBAND INTERFACE WITH POWER CONTROL"
Serial No.: 10/632,051
Attorney Docket No.: ST02009CIP1 (245-US-CIP1)

Please acknowledge receipt of the following documents:

1) Reinstatement Request and Supplemental Appeal Brief (25 pages).

CERTIFICATE OF TRANSMISSION

I hereby certify that this document (along with any papers referenced as being attached or enclosed) is being transmitted to the United States Patent and Trademark Office via facsimile to Fax No. (571) 273-8300, on the date set forth above.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Steve Gronemeyer DOCKET NO.: ST02009CIP1(245-US-CIP1)

SERIAL NO.: 10/632,051 GROUP ART UNIT: 2618

DATE FILED: July 30, 2003 EXAMINER: Nguyen, Duc M.

TITLE: SERIAL RADIO FREQUENCY TO BASEBAND INTERFACE WITH POWER CONTROL

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Mariana Paula Noli

THE ECLIPSE GROUP LLP
10605 Balboa Blvd., Suite 300
Granada Hills, CA 91344

January 21, 2009

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REINSTATEMENT REQUEST and SUPPLIMENTAL APPEAL BRIEF

Applicants now request reinstatement of their appeal and submit this Supplemental Appeal Brief in the above identified matter to reinstate and in support of the appeal to the Board of Patent Appeals and Interferences from the final rejections contained in the Final Office action dated August 6, 2007 and Advisory Action that was dated November 13, 2007, and most recently the Non-Final Office Action dated October 21, 2008 that reopened prosecution. Applicants filed the Notice of Appeal on February 6, 2008 along with a "Pre-Appeal Brief Request for Review" and on March 21, 2008 a "Notice of Panel Decision from Pre-Appeal brief Review" was issued indicating that there is at least one actual issue for appeal. After submission of the Appeal Brief that made the same arguments as the Pre-Appeal Brief, the Examiner issued a non-final office

action on October 21, 2008 and reopened prosecution. Applicants are currently facing the same references in the current application along with a provisional double patenting rejection in the Non-Final Office Action, so it is requested that the Appeal be reinstated. This Supplemental Appeal Brief is being submitted with the reinstatement request.

Serial No.: 11/632,051
Docket No.: ST02009CII (245-US-CIP1)

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is SiRF Technologies, Inc., assignee named in that certain Assignment recorded December 23, 2003 at Frame 014818, Reel 0651.

II. RELATED APPEALS AND INTERFERENCES

There are no prior or pending, judicial proceedings or interferences known to the Applicants that may be related to, directly effect or be directly effected by, or have a bearing on the Board of Patent Appeals and Interference's decision in the pending appeal.

This pending Appeal is being reinstated in response to the prosecution being reopened by the Examiner in the Non-Final Office action of October 21, 2008.

III. STATUS OF CLAIMS

This is an Appeal from the August 6, 2007, Final Office Action and Advisory Action of November 13, 2007, in which each of the pending claims 1-33 were rejected. Applicants are appealing the rejection of claims 1-33; and the reopened prosecution's Non-final Office Action of October 21, 2008, in which claims 1-20 and 22-33 now stand rejected, with claim 21 being objected to, and claims 1-33 being provisionally rejected due to a non-statutory double patenting rejection.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the mailing of the Advisory Action dated November 13, 2007. That Advisory Action indicated that the Final Office Action Response was entered by the Examiner.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention provides radio frequency (RF) power control messaging, as well as related methods of providing RF power control messaging, over an interface between an RF processing section and a baseband processing section. The interface supports general purpose bi-directional message transmission between the RF processing section and the baseband processing section. The interface further supports transmission of satellite positioning system (SPS) signal samples between the two processing sections without adding undue complexity to the interface.

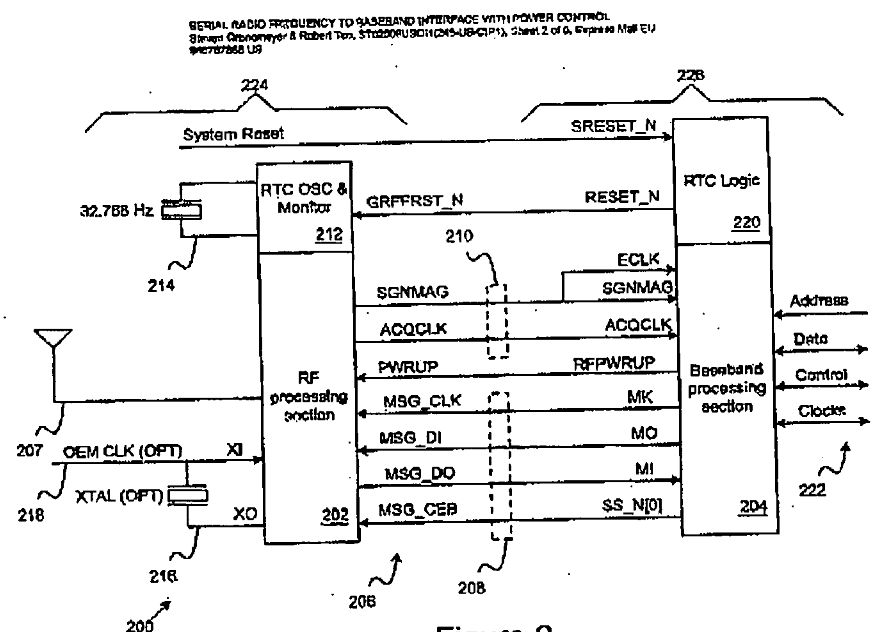

Figure 2

Referring to Figure 2 of the application (shown above), an interface 206 includes a message serial interface 208 and a data serial interface 210. The message serial interface 208 provides for serial communication of general purpose messages bi-

directionally between the RF section 202 and the baseband section 204. In contrast, the ARF section 202 employs the data serial interface 210 to transmit SPS signal samples to the baseband section 204.

The message serial interface 208, as shown in Figure 2, includes the message-in signal line (labeled MSG_DO/MI), a message-out signal line (Labeled MSG_DI/MO), a message clock signal line (MSG_CLK/MK), and a slave select signal line (labeled MSG_CEB/SS_N[0]). The labels on the message signal lines indicate the direction of data flow from the perspective of the RF section 202/baseband section 204. For example, the message-out signal line (MSG_DI/MO) carries message bits input to the RF section 202 and output by the base band section 204.

A power control signal (labeled PWRUP/RFPWRUP) may be provided to control whether certain portions of the RF section 202 are powered-up. The power control signal may be connected, for example, to a voltage regulator enabled pin in the RF section 202 to provide a coarse power-up/power-down control over the majority of the circuitry in the RF section 202. The RTC OSC & Monitor section 212 is separately powered so that it can continue to provide a clock to the baseband section 204. The baseband processing side may include an RTC logic section 220. The TRC logic section 220 accepts the input clock generated by the RTC OSC & Monitor section 212 as an aide in determining the current time as well as SPS location.

Messaging used by the serial interface for controlling the different portions of the RF chip 102 are shown in TABLE 4 on pages 19-21 of Applicants' patent application. TABLE 4 include messages for controlling power to the fractional N synthesizer, PLL and divider chain, first LNA, Oscillator, ACQCLK-Select mux and ACQCLK driver,

Front end power for 2nd low noise amplifier through A/D converter. Further, separate messages are for testing purposes, such as partition the reception chain in the RF section 202 for testing, specifying the synthesizer charge pump output and test modes, specifies the divider for PLL feedback.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.

Whether claims 1-13 are unpatentable under 35 U.S.C. §103(a) over Kerth et al. (US 2002/0132648) in view of Molnar (US 2002/0142741); whether claims 14-20 and 22-33 are unpatentable under 35 U.S.C. §103(a) over Kerth et al. (US 2002/0132648) in view of Molnar (US 2002/0142741) and further in view of Syrjarinne et al. (US 2003/0107514); whether claim 21 is properly objected to; and whether claims 1-33 are unpatentable over claims 1-60 due to non-statutory double patenting of co-pending Application No. 10/369,853 in view of Molnar (US 2002/0142741).

VII. ARGUMENT

Independent claims 1, 8, 14, 22, and 28 as currently presented, include the limitation of "a bi-directional message interface for communicating a power control message from the baseband section to the RF section that is associated with power consumption of the RF section." As noted in Applicants' Response filed October 9th, 2007, "the Kerth application states in paragraph [0096] that 'as noted above, the transceiver disables the transmitter circuitry during the receive mode of operation.' There is no mention or suggestion of power consumption in the Kerth application. More importantly, [the] Kerth application is not suggesting or teaching powering down the transmitter circuitry, but rather DISABLING the transmitter circuitry. Thus, one skilled in the art would not look to DISABLING the transmitter as being associated with power consumption. If anything, a person skilled in the art may look at the transceiver of the Kerth application as reusing some of the circuits for both transmitting and receiving while other circuits are disabled." (see Final Office Response dated October 9th, 2007, page 9, lines 14-21). Further, <u>the term "power control" does not even appear in the Kerth application</u>.

In response to Applicants' argument, the Examiner erroneously refers to the Kerth application as disclosing power control and states that "the Applicant[s] fails to provide reason or does not explain clearly why disabling the transmitter circuitry is NOT associated with power consumption. In fact, the Examiner asserts that disabling the transmitter circuitry is clearly associated with power consumption and would [be] equivalent to power down the transmitter circuitry..." (*see* page 2, Advisory Action mailed November 13, 2007, last paragraph).

The Examiner is reading "power control" into the Kerth application that is directed towards "reducing interference effects between the receiver analog circuitry and the receiver digital circuitry", (see abstract of the Kerth application). <u>There is no suggestion that the circuit is powered-down, only disabled.</u> This is shown in the Kerth application when a signal line is called a power-down (PBNB) signal in paragraph [0093] and defined to "configure the functionality of the interface signal lines... rather than using the PDNB signal, one may [use] other signals to control the configuration of the interface signal lines." There is just no explicit or even implicit teaching that the PDNB signal is being used to actually power down, or control the powering down of anything in the RF section.

Further, the Kerth application describes in paragraph [0094] that "[i]n the power-down or serial interface mode...the transceiver may also perform circuit calibration and adjustment procedures, as desired. For example, the values of various transceiver components may vary over time or among transceivers produced in different manufacturing batches. The transceiver may calibrate and adjust its circuitry to take those variations into account and provide higher performance." As explained in the Kerth application, the transceivers are not being powered down by the PDNB signal; rather they are switched out of the data path allowing calibration and adjustments to them.

The PDNB signal is also a unidirectional signal as taught in the Kerth application. Using claim 1 as an example, a "bi-directional message interface" is required. Since the PDNB signal is unidirectional it can not be equated with the bi-directional message interface element of the claims.

In summary, the Kerth application does not mention power control and nothing is powered down because Kerth describes the PDNB signal as a control signal to configure the functionality of the interface signal lines.

Therefore, if power control is not describe or taught by the Kerth application and it is not found in the Molnar application (which was not cited for power control), then the combination of the references fails to describe or teach all of Applicants' claim elements as currently presented and claims 1-13 are in condition for allowance.

The Syrjarine application was cited by the Examiner for disclosing a GPS receiver in a mobile phone. The Examiner goes on to state that Syrjarine also SUGGESTS a low power standby mode. The Examiner does not use Syrjarine for describing or teaching bi-directional message interface for communicating a power control message from the baseband section to the RF section. There is no power control that occurs between the baseband section and the RF section at all in the Syjarine patent. Thus, the teachings of this reference actually teach away from the claimed invention of bi-directional message interface for communicating a power control message from the baseband section to the RF section. Therefore, the claimed power control is not found in the Syrjarine reference either. So, the combination of the Kerth application in view of the Molnar application and in further view of the Syrjarine application, also fails to describe or teach all of Applicants' claim elements and claims 14-20 and 23-33 are in condition for allowance. Claim 21 depending from allowable independent claim 14 results in the objection to claim 21 being moot.

Turning to the non-statutory double patenting rejection, the Examiner is combing the parent with another reference. The Examiner admits the parent does not explicitly

teach the power control message is associated with power consumption of the RF section. Thus, the parent application's claims are different from the pending application. Further, the Examiner has not shown that the claims are not patentable distinct from the referenced claims. The Examiner only makes a general assertion along with an admission that the parent application's claims are different and proceeds to make an obviousness argument.

In order to establish double patenting, the Examiner must show [1] that "at least one examined application claim is not patentably distinct from the reference claim(s) [2] because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s)." See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed.Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993). The Examiner skipped the first prong and jumped right to the second prong in an attempt to show non-statutory double patenting. Therefore, the provisional rejection of claims 1-33 is in proper because the Examiner has not shown that the claims are not patentable distinct.

VIII. Conclusion

For the reasons stated above, Applicants respectfully submit that claims 1-33 as presented are in condition for allowance because not all claim elements are taught or described in the combined references, there is no likelihood of success in combining the elements to achieve the claimed invention, and there is no suggestion to combine the references when the resulting device would be missing claim elements.

Respectfully submitted by
Attorney for Applicants

Gregory B. Gulliver

GREGORY B. GULLIVER
Reg. No. 44,138
Phone: (847) 282-3551
Fax: (949) 608-3645

The Eclipse Group LLP
10605 Balboa Blvd., Suite 300
Granada Hills, CA 91344

IX. CLAIMS - APPENDIX

1. (Previously presented) A radio frequency (RF) to baseband interface providing power control over an RF section that processes RF signals and that is coupled to a baseband section that processes baseband signals, the interface comprising:

a bi-directional message interface for communicating a power control message from the baseband section to the RF section that is associated with power consumption of the RF section; and

a data interface for communicating data from the RF section to the baseband section.

2. (Original) The interface of claim 1, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF section.

3. (Original) The interface of claim 2, where the power state is one of a power-up state and a power-down state.

4. (Original) The interface of claim 1, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

5. (Original) The interface of claim 2, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

6. (Original) The interface of claim 1, where the message interface is a serial message interface.

7. (Original) The interface of claim 1, where the message interface comprises a message-in signal line, a message-out signal line and a message clock signal line.

8. (Previously presented) A method for controlling power in a radio frequency (RF) section that processes RF signals and that is coupled to a baseband section that processes baseband signals, the method comprising the steps of:

setting a power control bit in a power control message; and

communicating the power control message over a message interface from the baseband section to the RF section where the power control message is associated with power consumption of the RF section.

9. (Original) The method of claim 8, wherein the step of communicating comprises the step of serially communicating the power control message.

10. (Original) The method of claim 8, wherein the step of communicating comprises the step of serially communicating the power control message using a message-in signal line, a message-out signal line and a message clock signal line.

11. (Original) The method of claim 8, where the power control bit specifies a power state for pre-selected circuitry in the RF section.

12. (Original) The method of claim 11, where the power state is one of a power-up state and a power-down state.

13. (Original) The method of claim 8, where the step of setting comprises the step of setting a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

14. (Previously presented) An RF front end for a satellite positioning system receiver, the front end comprising:

an RF processing section comprising an RF input for receiving satellite positioning system signals; and

an RF to baseband interface coupled to the RF processing section, the interface comprising:

a bi-directional message interface for communicating messages between the RF processing section and a baseband processing section, including receiving a power control message from the baseband processing section wherein the power control message is associated with power consumption of the RF processing section; and

a data interface for communicating data from the RF processing section to the baseband processing section.

15. (Original) The RF front end of claim 14, wherein the message interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

16. (Original) The RF front end of claim 15, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF section.

17. (Original) The RF front end of claim 16, where the power state is one of a power-up state and a power-down state.

18. (Original) The RF front end of claim 15, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

19. (Original) The RF front end of claim 15, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

20. (Original) The RF front end of claim 15, where the data interface comprises a data clock signal line and a data bit signal line.

21. (Original) The RF front end of claim 20, where:

the data clock signal line carries a data clock comprising a rising edge and a falling edge;

the data bit signal line carries a data signal comprising a sign bit and a magnitude bit; and

the first data bit is valid on the rising edge of the data clock and the second data bit is valid on the falling edge of the data clock.

22. (Previously presented) A baseband back end for a satellite positioning system receiver, the back end comprising:

a baseband processing section comprising at least one address, data, and control line for communicating with a digital device; and

an RF to baseband interface coupled to the baseband processing section, the interface comprising:

a bi-directional message interface for communicating messages between an RF processing section and the baseband processing section, including communicating a power control message to the RF processing section where the power control message is associated with power consumption of the RF processing section; and

a data serial interface for communicating data from the RF processing section to the baseband processing section.

23. (Original) The baseband back end of claim 22, wherein the message serial interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

24. (Original) The baseband back end of claim 22, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF processing section.

25. (Original) The baseband back end of claim 24, where the power state is one of a power-up state and a power-down state.

26. (Original) The baseband back end of claim 22, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

27. (Original) The baseband back end of claim 26, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

28. (Previously presented) A satellite positioning system receiver comprising:

an RF front end comprising an RF processing section and an RF input for receiving satellite positioning system signals;

a baseband back end comprising a baseband processing section and at least one address, data, and control line for communicating with a digital device; and

an RF to baseband interface coupled between the RF processing section and the baseband processing section, the interface comprising:

a bi-directional message interface for communicating messages between the RF processing section and the baseband processing section, including communicating a power control message to the RF processing section where the power control message is associated with power consumption of the RF processing section; and

a data interface for communicating data from the RF processing section to the baseband processing section.

29. (Original) The satellite positioning system receiver of claim 28, wherein the message interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

30. (Original) The satellite positioning system receiver of claim 29, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF processing section.

31. (Original) The satellite positioning system receiver of claim 30, where the power state is one of a power-up state and a power-down state.

32. (Original) The satellite positioning system receiver of claim 29, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

33. (Original) The satellite positioning system receiver of claim 32, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

X. EVIDENCE – APPENDIX

No Evidence Appendix is included.

XI. RELATED PROCEEDINGS – APPENDIX

None.